

## 11.1 A 48-to-860MHz CMOS Direct-Conversion TV Tuner

M. Gupta<sup>1</sup>, S. Lerstaveesin<sup>1</sup>, D. Kang<sup>1</sup>, B-S. Song<sup>2</sup>

<sup>1</sup>Chrontel, San Diego, CA

<sup>2</sup>University of California at San Diego, La Jolla, Ca

Many of the existing analog/digital terrestrial/cable TV standards such as NTSC, PAL, ATSC, and DVB use a wide VHF/UHF frequency range from 48 to 860MHz. This broadband nature of the TV band introduces many technical challenges in the design of silicon tuners. These design challenges include harmonic reject mixing, image rejection, low noise and linearity over wide bandwidth, and high dynamic range. Either RF tracking filter or up/down dual conversion [1] has been used to avoid the harmonic mixing problem. The external SAW filters are used to attenuate the image channels, which can be 30 to 40dB stronger than the desired channel. A more integrated TV tuner architecture uses selectable on-chip RF bandpass filters for suppression of odd harmonics of the LO and polyphase filters for image suppression [2]. It requires high power for active filtering, and the in-band image rejection is still limited by the I/Q path matching. This work uses a simple on-chip RF tunable bandpass filter and polyphase mixer for harmonic rejection. Image rejection and channel filtering are implemented digitally [3].

In the double-quadrature mixing, the complex LO carrier is ideally a single tone at  $-f_{LO}$ . In a traditional Gilbert-type mixer, due to inherent current switching controlled by the LO, the mixing operation effectively generates the odd harmonics of the LO with magnitudes of 1/3, 1/5, 1/7, and so on, but alternately at positive and negative frequencies, that is, at  $+3f_{LO}$ ,  $-5f_{LO}$ ,  $+7f_{LO}$ , etc. Also, the LO I/Q mismatch creates image components at negative frequencies, e.g.,  $+f_{LO}$ ,  $-3f_{LO}$ ,  $+5f_{LO}$ , and  $-7f_{LO}$ . Similarly, the complex RF signal has a negative-frequency spectrum due to the I/Q mismatch. Therefore, in the downconversion process to low or zero IF, the undesired TV bands are folded into the desired signal band. If an ideal double-quadrature mixing is used, the effect of the 3<sup>rd</sup> and 7<sup>th</sup> harmonics is greatly reduced [2]. One way of further reducing the effect of odd harmonics is by using a polyphase mixer [4]. Polyphase mixing relies on cancellation of the odd harmonics of the LO by using vector sum arithmetic. For example, when the fundamental LO signal shifts by 45° and 90°, the 3<sup>rd</sup> harmonics of the LO signal shifts three times more by 135° and 270°, leading to the cancellation of the 3<sup>rd</sup> and similarly of the 5<sup>th</sup> harmonics, and the constructive summation of the signal. However, the suppression of harmonics due to the polyphase mixing is usually limited to around 30dB because of the gain and phase errors. To achieve additional suppression of undesired harmonic mixing, a tunable RF filter is needed to suppress the TV signal bands at odd harmonics by at least an additional 30dB before the polyphase mixing. In theory, the double-quadrature mixing also significantly reduces the effect of the image leakage, but is still limited by the I/Q mismatches.

The proposed TV tuner architecture is shown in Fig. 11.1.1. The broadband front-end contains a noise-canceling amplifier and an attenuator shown in Fig. 11.1.2. It has a combined programmable gain range of 30 to -40dB with a 0.85dB step, and provides a wideband input impedance matching. The RF tracking filter shown in Fig. 11.1.3 is a 4<sup>th</sup>-order filter using the coupled-resonator topology. As a result, the RF filter also generates a quadrature RF signal, which is then used for a complex polyphase LO. The PLL uses three VCOs to generate frequencies from 1.1 to 2.2GHz. These frequencies are then divided down to cover the TV band from 48 to 860MHz. The capacitors of the VCO are self-calibrated for operation in the linear VCO gain region. The LO directly downconverts the desired channel to a low IF (for example, 4.57MHz). The polyphase mixer is implemented by splitting

a typical Gilbert-type mixer into three individual mixers with voltage gain ratio of 1:1.4:1 [4]. A 10<sup>th</sup>-order RC low-pass anti-aliasing filter has a bandwidth of 10MHz. The capacitors of this filter are also self-calibrated using a master/slave tuning. The VGA after the filter has a gain range from 0 to 20dB with a step size of 1.25dB. Two 11b pipelined ADCs are used for I/Q signals. A complex channel-select filter is made programmable for 6-to-8MHz bandwidth. The image rejection is performed digitally using 1-tap LMS noise-cancellation scheme in the baseband [3]. The proposed system has a low-IF complex (I/Q) digital output. A digital Hilbert filter is used to convert the complex baseband signal into a real bandpass signal, which is then converted into an analog output using a 10b DAC. The only external components are a 27MHz crystal and loop filter capacitors.

The prototype chip, fabricated in a 0.18μm CMOS technology, occupies 5×5mm<sup>2</sup>, and consumes 750mW from a single 1.8V supply. The analog portion of the chip consumes about 540mW. The measured system NF varies from 4 to 7dB at 30dB LNA gain. The AGC has a total gain range of 90dB. The RF filter has 7dB NF with a nominal gain of 8dB. The RF filter has 16 tunable bands. Figure 11.1.5 shows harmonic and image rejections are better than 72 and 61dB, respectively, when measured with harmonic and image stronger than the desired channel by 30dB. The in-band VCO phase noise of the synthesizer is measured to be -90dBc/Hz at 10kHz offset. However, after the VCO frequency is divided for the polyphase LO, the effective integrated phase noise is in the range of 0.05 to 0.8° depending on the TV band. MOS caps are used for VCO tuning and control, and the VCO gain is set to below 40MHz/V. The PLL loop bandwidth is 100kHz. The measured midband sensitivity of the tuner for 8-VSB ATSC signal is -86dBm for BER less than 10<sup>-3</sup> before the Reed-Solomon decoder. For the similar BER specification, the sensitivity of the tuner is measured to be -79dBm for J.83/B cable TV standard when 64-QAM is used. Figure 11.1.6 shows a demodulated 256-QAM constellation from an actual TV cable for J.83/B standard achieving more than 31.5dB MER and 35.8dB EVM. In the 8-VSB mode, the tuner takes 40dB and 57dB stronger NTSC blockers at N±1 and N±6 channels, respectively. Measured performance is summarized in Fig. 11.1.6, and a die micrograph is shown in Fig. 11.1.7.

### References:

- [1] M. Dawkins, A. Burdett, and N. Cowley, "A Single-Chip Tuner for DVB-T," *IEEE J. of Solid-State Circuits*, vol. 38, pp. 1307-1317, Aug., 2003.
- [2] J. van Sinderen, F. Seneschal, E. Stikvoort, F. Mounaim, M. Notten, H. Brekelmans, O. Crand, F. Singh, M. Bernard, V. Fillatre, and A. Tombeur, "A 48-860MHz Digital Cable Tuner IC with Integrated RF and IF Selectivity," *ISSCC Dig. Tech. Papers*, pp. 444-445, Feb., 2003.
- [3] C. Heng, M. Gupta, S. Lee, D. Kang, and B. Song, "A CMOS TV Tuner/Demodulator IC With Digital Image Rejection," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2525-2535, Dec., 2005.
- [4] J. Weldon, R. Narayanaswami, J. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K. Tsai, C. Lee, and P. Gray, "A 1.75-GHz Highly Integrated Narrow-Band CMOS Transmitter with Harmonic-Rejection Mixers," *IEEE J. Solid-State Circuits*, pp. 2003-2015, vol. 36, Dec., 2001.

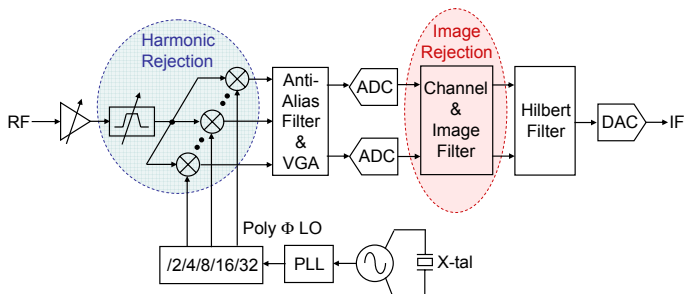


Figure 11.1.1: Direct-conversion TV tuner architecture.

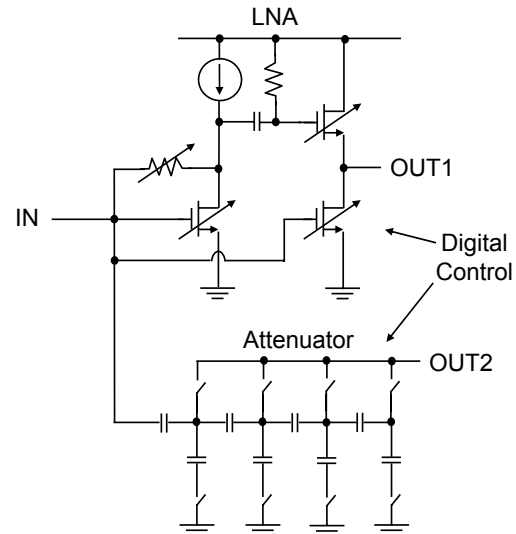


Figure 11.1.2: Schematic of the first-stage LNA/attenuator.

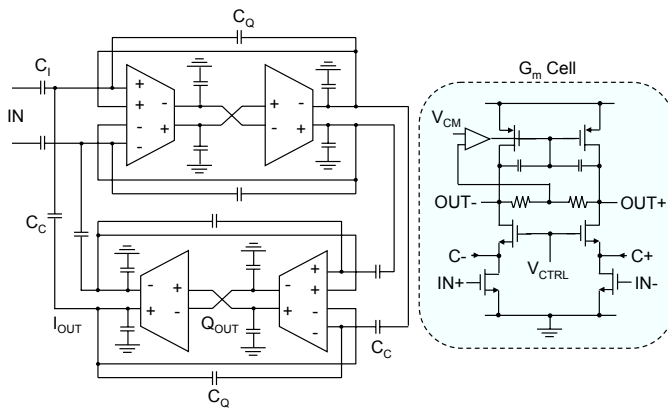
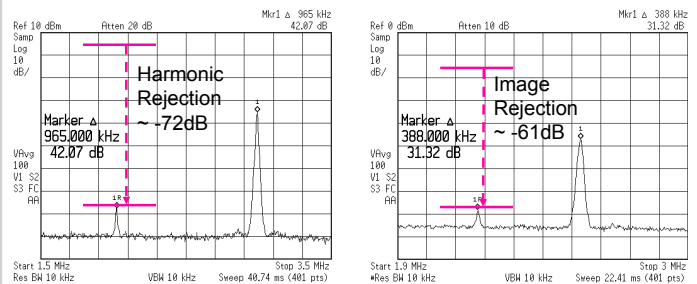
Figure 11.1.3: Block diagram of the coupled-resonator RF filter with linear  $G_m$  cell.

Figure 11.1.4: Harmonic and image rejections.

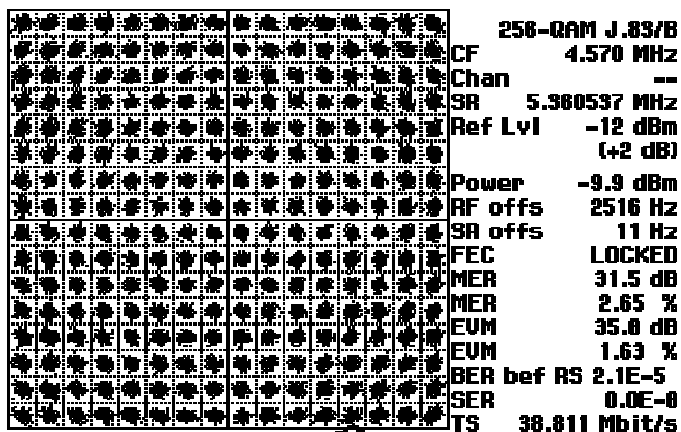


Figure 11.1.5: Demodulated constellation of actual 256-QAM cable signal.

Frequency Range	48 to 860MHz
Sensitivity	-79dBm (64-QAM, MER 22dB) -86dBm (8-VSB, MER 15dB)
Total AGC Gain Range	90dB
Noise Figure	4 to 7dB @ max gain
Harmonic/Image Rejection	72/61dB (30dB stronger harmonic & image)
IIP3 (@ 500MHz)	17.5/10/-13.8dBm (min/0/max LNA gain)
IIP2 (@ 500MHz)	36.5/17.1/-22.4dBm (min/0/max LNA gain)
$P_{1dB}$ (@ 500MHz)	8/0.5/-23.5dBm (min/0/max LNA gain)
CTB, CSO, XMOD	-53, -115, -70dBc (min LNA gain)
VSWR	1.8 to 2.8dB ( $S_{11} = -11$ to $-6.6$ dB)
LO Range	1.1 to 2.2GHz
LO Phase Noise	~-90dBc/Hz @ 10kHz Offset
Divided LO RMS Phase Noise	0.05 to 0.8° within 10kHz to 10MHz
Die Area	5x5mm <sup>2</sup> in 0.18μm CMOS
Power	750mW @ 1.8V

Figure 11.1.6: Measured performance summary.

Continued on Page 597

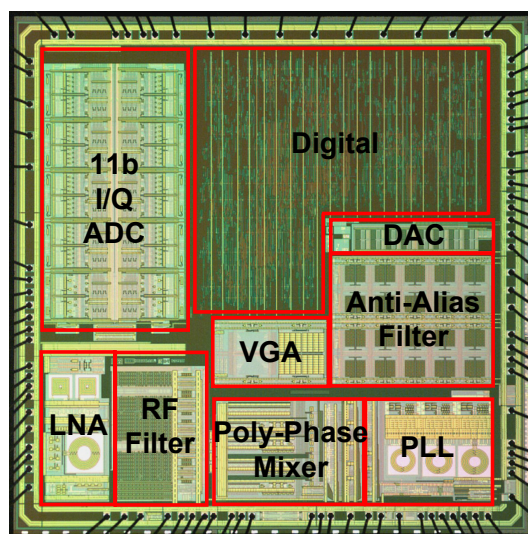


Figure 11.1.7: Die micrograph.